WHAT IS CLAIMED IS:

1. An interconnection network for routing data packets comprising:

eight switching circuits capable of transferring data packets with each other;

eight sequential data links bidirectionally coupling said eight switching circuits in sequence to thereby form an octagonal ring configuration; and

four crossing data links, wherein a first crossing data link bidirectionally couples a first switching circuit to a fifth switching circuit, a second crossing data link bidirectionally couples a second switching circuit to a sixth switching circuit, a third crossing data link bidirectionally couples a third switching circuit to a seventh switching circuit, and a fourth crossing data link bidirectionally couples a fourth switching circuit to an eighth switching circuit.

2. The interconnection network as set forth in Claim 1 wherein a first data packet may be transmitted from a source switching circuit to a destination switching circuit in no more than two data transfers between any of said eight switching circuits.

3. The interconnection network as set forth in Claim 1 wherein said first switching circuit has switch address 0 (S0), said second switching circuit has switch address 1 (S1), said third switching circuit has switch address 2 (S2), said fourth switching circuit has switch address 3 (S3), said fifth switching circuit has switch address 4 (S4), said sixth switching circuit has switch address 5 (S5), said seventh switching circuit has switch address 6 (S6), and said eighth switching circuit has switch address 7 (S7).

4. The interconnection network as set forth in Claim 3 wherein each of said eight switching circuits is associated with a processing node capable of processing said data packets.

5. The interconnection network as set forth in Claim 4 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to a next sequential one of said eight switching circuits having switch address S(i+1) (modulo 8) if a destination switch address associated with said received data packet exceeds said switch address S(i) of said selected switching circuit by no more than 2.

6. The interconnection network as set forth in Claim 4 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to a preceding sequential one of said eight switching circuits having switch address S(i-1) (modulo 8) if said switch address S(i) of said selected switching circuit exceeds a destination switch address associated with said received data packet by no more than 2.

7. The interconnection network as set forth in Claim 4 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to a selected processing node associated with said selected switching circuit if said switch address S(i) of said selected switching circuit is equal to a destination switch address associated with said received data packet.

8. The interconnection network as set forth in Claim 4 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to an opposing one of said eight switching circuits having switch address S(i+4) (modulo 8) if a destination switch address associated with said received data packet exceeds said switch address S(i) of said selected switching circuit by more than 2.

9. A system-on-a-chip (SOC) device comprising:

eight processing nodes; and

an interconnection network for transferring data packets between said eight processing nodes, said interconnection network comprising:

eight switching circuits capable of transferring data packets with each other, wherein each of said eight switching circuits is associated with one of said eight processing nodes;

eight sequential data links bidirectionally coupling said eight switching circuits in sequence to thereby form an octagonal ring configuration; and

four crossing data links, wherein a first crossing data link bidirectionally couples a first switching circuit to a fifth switching circuit, a second crossing data link bidirectionally couples a second switching circuit to a sixth switching circuit, a third crossing data link bidirectionally couples a third switching circuit to a seventh switching circuit, and a fourth crossing data link bidirectionally couples a fourth switching circuit to an eighth switching circuit.

10. The system-on-a-chip (SOC) device as set forth in Claim 9 wherein a first data packet may be transmitted from a source switching circuit to a destination switching circuit in no more than two data transfers between any of said eight switching circuits.

11. The system-on-a-chip (SOC) device as set forth in Claim 9 wherein said first switching circuit has switch address 0 (S0), said second switching circuit has switch address 1 (S1), said third switching circuit has switch address 2 (S2), said fourth switching circuit has switch address 3 (S3), said fifth switching circuit has switch address 4 (S4), said sixth switching circuit has switch address 5 (S5), said seventh switching circuit has switch address 6 (S6), and said eighth switching circuit has switch address 7 (S7).

12. The system-on-a-chip (SOC) device as set forth in Claim 11 wherein each of said eight processing node is capable of processing said data packets.

13. The system-on-a-chip (SOC) device network as set forth in Claim 12 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to a next sequential one of said eight switching circuits having switch address S(i+1) (modulo 8) if a destination switch address associated with said received data packet exceeds said switch address S(i) of said selected switching circuit by no more than 2.

14. The system-on-a-chip (SOC) device as set forth in Claim 12 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to a preceding sequential one of said eight switching circuits having switch address S(i-1) (modulo 8) if said switch address S(i) of said selected switching circuit exceeds a destination switch address associated with said received data packet by no more than 2.

15. The system-on-a-chip (SOC) device as set forth in Claim 12 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to a selected processing node associated with said selected switching circuit if said switch address S(i) of said selected switching circuit is equal to a destination switch address associated with said received data packet.

16. The system-on-a-chip (SOC) device as set forth in Claim 12 wherein a selected one of said eight switching circuits having switch address S(i) transfers a received data packet to an opposing one of said eight switching circuits having switch address S(i+4) (modulo 8) if a destination switch address associated with said received data packet exceeds said switch address S(i) of said selected switching circuit by more than 2.

17. A system-on-a-chip (SOC) device comprising:

a plurality of processing nodes;

a first interconnection network for transferring data packets between first selected ones of said plurality of processing nodes;

a second interconnection network for transferring data packets between second selected ones of said plurality of processing nodes; wherein each of said first and second interconnection networks comprises:

eight switching circuits capable of transferring data packets with each other, wherein each of said eight switching circuits is associated with one of said plurality of processing nodes;

eight sequential data links bidirectionally coupling said eight switching circuits in sequence to thereby form an octagonal ring configuration; and

four crossing data links, wherein a first crossing data link bidirectionally couples a first switching circuit to a fifth switching circuit, a second crossing data link bidirectionally couples a second switching circuit to a sixth switching circuit, a third crossing data link bidirectionally couples a third switching circuit to a seventh switching

circuit, and a fourth crossing data link bidirectionally couples a fourth switching circuit to an eighth switching circuit; and.

18. The system-on-a-chip (SOC) device as set forth in Claim 17 wherein a first data packet may be transmitted from a source switching circuit to a destination switching circuit in no more than two data transfers between any of said eight switching circuits in said first interconnection network.

19. The system-on-a-chip (SOC) device as set forth in Claim 18 wherein a second data packet may be transmitted from a source switching circuit to a destination switching circuit in no more than two data transfers between any of said eight switching circuits in said second interconnection network.

20. The system-on-a-chip (SOC) device as set forth in Claim 19 wherein one of said eight switching circuits in said first interconnection network and one of said eight switching circuits in said second interconnection network are the same switching circuit.

21. A method of transferring data in an interconnection network comprising: 1) eight switching circuits capable of transferring data packets with each other; 2) eight sequential data links bidirectionally coupling the eight switching circuits in sequence to thereby form an octagonal ring configuration; and 3) four crossing data links, wherein a first crossing data link bidirectionally couples a first switching circuit to a fifth switching circuit, a second crossing data link bidirectionally couples a second switching circuit to a sixth switching circuit, a third crossing data link bidirectionally couples a third switching circuit to a seventh switching circuit, and a fourth crossing data link bidirectionally couples a fourth switching circuit to an eighth switching circuit, the method comprising the steps of:

receiving a data packet in a selected one of the eight switching circuits having switch address S(i); and

transferring the received data packet to a next sequential one of the eight switching circuits having switch address S(i+1) (modulo 8) if a destination switch address associated with the received data packet exceeds the switch address S(i) of the selected switching circuit by no more than 2.

22. The method of transferring data as set forth in Claim 21 wherein the selected switching circuit having switch address S(i) transfers the received data packet to a next sequential one of the eight switching circuits having switch address S(i+1) (modulo 8) if the destination switch address exceeds the switch address S(i) of the selected switching circuit by no more than 2.

23. The method of transferring data as set forth in Claim 22 wherein the selected switching circuit having switch address S(i) transfers the received data packet to a preceding sequential one of the eight switching circuits having switch address S(i-1) (modulo 8) if the switch address S(i) of the selected switching circuit exceeds the destination switch address by no more than 2.

24. The method of transferring data as set forth in Claim 23 wherein the selected switching circuit transfers the received data packet to a selected processing node associated with the selected switching circuit if the switch address S(i) of the selected switching circuit is equal to the destination switch address.

25. The method of transferring data as set forth in Claim 24 wherein the selected switching circuit transfers the received data packet to an opposing one of the eight switching circuits having switch address S(i+4) (modulo 8) if the destination switch address exceeds the switch address S(i) of the selected switching circuit by more than 2.